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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	09/944,234	ZAGREBELNY ET AL.
	Examiner	Art Unit
	Hsien-Ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,12-16 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,12-16 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The advisory action mailed 3/1/2004 is withdrawn. The Final rejection mailed 7/28/03 is withdrawn.

2. Applicant's cancellation to claims 3, 9-11 and 17-23 is acknowledged. Thus, claims 1-2, 4-8, 12-16 and 24-26 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4, 5, 12-16 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,484,300) in view of Saka et al. (US 6,476,921).

In re claims 1, 2, 4, and 5, Kim et al. teach the claimed method of making a semiconductor structure, comprising:

- calculating a pattern density and measuring a thickness of a layer 530 to be polished, measuring the thickness being X1 (Fig.5A and col. 10, lines 3-63);
- identifying a composition of the layer, i.e. identifying the composition being silicon oxide (col.12, lines 29-34);
- calculating a first polish time sufficient to planarize a layer 530 on a semiconductor substrate 510, i.e. calculating a first polish time enough to polish the layer 530 from

thickness X1 down to a predetermined thickness by computer simulation, prior to reaching thickness X2 (Fig.5A) (abstract, col.10, line 64 through col. 11, line 11);

- determining a second polish time sufficient to reduce the thickness of the layer 530 after planarization to the predetermined thickness and polishing the layer 530 for the second polish time, i.e. determining a time enough to polish the layer 530 from the predetermined thickness down to thickness X2 based on computer simulation and polishing the layer 530 for the second time to reach the thickness X2 (Fig.5A and col. 16, claim 10);
- polishing the layer 530 for said first polish time to planarize the layer 530 from a thickness X1 as shown in Fig.5A; and
- polishing the layer 530 to a predetermined thickness (i.e. down to thickness X2 as shown in Fig.5A).

In re claims 13-16, Kim et al. also teach making a semiconductor structure as shown in Fig.5A by the method and forming a semiconductor device and an electronic device comprising the semiconductor device (i.e. integrated circuit device) from the structure (col. 14, lines 49-56).

In re claims 24-26, Kim et al. further teach the claimed method, comprising: polishing a layer 530 on a semiconductor substrate 510 with a system comprising a chemical mechanical polishing apparatus and machine readable medium, comprising code, imbedded in the machine readable medium, for calculating a first polish time, sufficient to planarize a layer 530 on a substrate 510 (Figs. 3A-3C and col. 19, claim 29) and forming an electronic device comprising a semiconductor device, as stated above.

In re claims 1-2, 4, 5, 13-16 and 24-26, the **only** difference is that Kim et al. teach *calculating* the pattern density in the polishing method (i.e. CMP), whereas the instant invention recites *measuring* pattern density.

Saka et al., however, in an analogous art of polishing method (i.e. CMP), teach using a fiber optic reflectance system to transmit light from a light source to measure topography of an uneven surface (col. 5, lines 24-38). The topography is obtained from measuring the reflectance of the uneven surface (col. 5, lines 39-46). The measured reflectance is influenced by pattern density (col. 5, lines 18-21).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use the fiber optic reflectance system to measure pattern density, as taught by Saka et al., in the polishing method of Kim et al., since measuring pattern density would provide more accurate data than that of calculating pattern density, which would improve an accuracy of polishing.

In re claim 12, Kim et al. in view of Saka et al. teach the claimed method of making a semiconductor structure, including measuring the pattern density of the layer and calculating a first polish time sufficient to make the layer planar, as stated above, but do not expressly teach polishing for a third polish time equal to the sum of the first and second polish times.

However, the selection of the third polish time is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the

third polish time depends on the desired final thickness of the layer, pattern density and composition of the layer. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05, III

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US '300) in view of Saka et al. as applied to claims 1-2, 4, 5, 12-16 and 24-26 above and further in view of Maekawa (US 6,351,723).

In re claims 6 and 7, Kim et al. in view of Saka et al. substantially teach the claimed method as stated above but fail to teach that a Cpk of the method is at least 1.

However, Maekawa teaches that the Cpk value (a value of a deviation process capability) has been monitored in CMP process, wherein the Cpk value needs to be controlled at least 1 to obtain a sufficient process capability (col.6, lines 47-67).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to diagnose and control the Cpk value at least 1, as taught by Maekawa, during the CMP of Kim et al. in view of Saka et al. for the purpose of preventing the process from failure (see abstract, Maekawa).

In re claim 8, Kim et al. in view of Saka et al. and Maekawa teach the making of each semiconductor structure comprise, prior to calculating of the first polish time, measuring the thickness of the layer 530, a pattern density of the layer 530 and identifying a composition of the layer 530, as stated above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

March 27, 2004

Lee